

U.S.S.N. 10,788,702

**Specification Amendments**

Please replace paragraph 0010 with the following re-written paragraph:

A typical conventional CMP apparatus 90 is shown in FIG. 1 and includes a base 100; polishing pads 210a, 210b, and 210c provided on the base 100; a head clean load/unload (HCLU) station 360 which includes a load cup 300 for the loading and unloading of wafers (not shown) onto and from, respectively, the polishing pads; and a head rotation unit 400 having multiple polishing ~~pads~~ heads 410a, 410b, 410c and 410d for holding and fixedly rotating the wafers on the polishing pads.

Please replace paragraph 0025 with the following re-written paragraph:

In another embodiment, the metrology tool is interposed between the first polishing pad and the second polishing pad. The material layer on each of multiple wafers is then subjected to a first polishing step on the first polishing pad, a metrology step to measure the thickness of the layer, and to second and third polishing steps, respectively. In the second and third polishing steps, the layer is polished to the desired target

U.S.S.N. 10,788,702

thickness. The ~~build~~ in-line metrology can provide not only the final fine polish desired amount but also to feed backward the optimal polish condition for prior polished step or steps of successive wafers by adjusting process time, pressure, head/platen rotation speed and slurry flow.

Please replace paragraph 0039 with the following re-written paragraph:

Referring next to Figure 3A, the CMP apparatus 10 is used to polish and reduce the thickness of a material layer 27 ~~or 27 and 25~~ previously deposited on a wafer 26. Throughout the CMP polishing process, the material layer 27 ~~or 25~~ is reduced from a pre-CMP thickness 42, to a target thickness 44. Typically, the material layer 27 includes a metal layer on which is provided a dielectric layer 25. For example, the metal layer may be tungsten, copper or aluminum, or alloys of those metals, with an oxide dielectric layer provided thereon. The metal layer and the dielectric layer may be deposited on the wafer 26 using techniques such as PVD (physical vapor deposition), CVD (chemical vapor deposition) or ECP (electric chemical plating), for example. Alternatively, the entire material layer 27 ~~and 25~~ may

U.S.S.N. 10,788,702

be a dielectric layer[[s]], as in STI application.

Please replace paragraph 0043 with the following re-written paragraph:

After the first polishing step is completed, the head rotation unit 14 rotates the wafer 26 from the first polishing pad 28a to the second polishing pad 28b and rotates the material layer 27 against the second polishing pad 28b in a second polishing step, as indicated in step S4. The process controller 36 transmits a process signal 37b to the CMP apparatus 10, as shown in Figure [[5]]3. The head rotation unit 14 causes the polishing head to rotate the material layer 27 against the second polishing pad 28b for a time which depends on the estimated total polish time remaining, the pre-CMP thickness 42 and the target thickness 44 of the material layer 27 previously programmed into the process controller 36 at process step S1. Like the first polishing step, the second polishing step is typically a course polishing step in which material is removed from the material layer 27. Depending on the application, the course removal thickness may vary from 0~20,000 angstroms and the removal

U.S.S.N. 10,788,702

process is divided among two or more platens. The course polishing step may remove the cap layer only without contacting the underlying layer (0 angstroms), as in typical dual damascene applications. In other cases, the course polishing step may remove the cap layer in addition to underlying layer or layers, up to a depth of typically about 20,000 angstroms, such as in an IMD process.

Please replace paragraph 0044 with the following re-written paragraph:

After the second polishing step is completed, the head rotation unit 14 transfers the wafer 26 from the second polishing pad 28b to the in-line metrology tool 34. As indicated in step S5, at the in-line metrology tool 34, the thickness of the material layer 27 is measured. Other parameters, such as film density and sheet resistance ( $R_s$ ), may also be measured. As shown in Figures 3 and 5, the metrology tool 34 transmits a feedback signal 46, which corresponds to the measured thickness of the material layer 27 ~~or 25~~, to the process controller 36, in order to adjust the course polish conditions such as polish time, down force, platen/head rotation speed and slurry flow for the

U.S.S.N. 10,788,702

successive wafers. Based on the measured thickness of the material layer 27 ~~or 25~~, as indicated through the feedback signal 46, the process controller 36 calculates the time required to polish the material layer 27 ~~or 25~~ from the measured thickness to the intermediate target thickness 44, and transmits this information, through an adjustment signal 48, to the first and second polishing pads 28a, 28b, respectively, of the CMP apparatus 10 for the successive wafers to minimize the fine polish variation.

Please replace paragraph 0045 with the following re-written paragraph:

On the other hand, based on the measured thickness of the material layer 27 ~~or 25~~, as indicated through the feedback signal 46, the process controller 36 calculates the time required to polish the material layer 27 ~~or 25~~ from the measured thickness to the target thickness 44, and transmits this information, through an adjustment signal 48, to the third polishing pad 28c of the CMP apparatus 10. As indicated in process step S6, the third polishing pad 28c then polishes the material layer 27 from the measured thickness down to the target thickness 44, according to

U.S.S.N. 10,788,702

the calculated polishing time transmitted through the adjustment signal 48. Finally, the post-CMP thickness of the material layer 27 may then be measured to verify the target thickness before or after cleaning. As indicated in step S7, the wafer 26 may be subjected to a post-CMP cleaning process to remove particles remaining on the wafer 26, prior to continued semiconductor fabrication. This is carried out using the in-situ polish clean tool 50, or alternatively, the ex-situ polish clean tool 51. In the event that the measured post-CMP thickness deviates from the target thickness, the wafer 26 may be re-worked and subjected to another polishing and measuring cycle through the CMP apparatus 10.

Please replace paragraph 0046 with the following re-written paragraph:

As a first wafer 26 is polished on the first polishing pad 28a, a second wafer 26 is loaded onto the load/unload station 22.

The first wafer 26 is then transferred to and polished on the second polishing pad 28b, while the second wafer 26 is transferred to and polished on the first polishing pad 28a and a third wafer 26 is transferred to the load/unload station 22. The

U.S.S.N. 10,788,702

first wafer 26 is subjected to metrology at the metrology tool 34 while the second wafer 26 is polished at the second polishing pad 28b and the ~~first~~ third wafer 26 is polished at the first polishing pad 28a. The first wafer 26 is subjected to the final polishing step at the third polishing pad 28c while the second wafer 26 undergoes metrology at the metrology tool 34 and the third wafer 26 is polished at the second polishing pad 28b. Accordingly, multiple wafers 26 in a lot are sequentially polished throughout the polishing sequence.